Problem 7: **Calculate the gate capacitance with an oxide capacitance of $C_{ox} = 3.45 \times 10^{-7}$ F/cm^2 and a gate with dimensions $W = 8$ µm and $L = .5$ µm**

Solution:

$$C_g = C_{ox} \cdot A \quad \text{where } A = WL$$

$$= 3.45 \times 10^{-7} \times 8 \times 10^{-4} \times .5 \times 10^{-4}$$

$$= 13.8 \times 10^{-15}$$

$$= 13.8 \text{ fF}$$

The gate-source and gate-drain contribution are then estimated by

$$C_{gs} = 1/2 C_g$$

$$= 6.9 \text{ fF}$$

Problem 11: **Consider the nMOS transistor in a 180 nm process with a nominal therehold voltage of 0.4 V and doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1 V instead of 0 V? $\varepsilon_{si} = 11.7 \times 8.85 \times 10^{-14}$ F/cm**

Solution: $V_{sb} = 1.1$

$$V_t = V_{to} + \gamma\left(\sqrt{2\,\phi_b + |V_{sb}|} - \sqrt{2\,\phi_b}\right)$$

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\,\varepsilon_{si}\cdot N_A}$$

$$V_{to} = 2\,\phi_b + \frac{\sqrt{2q\,\varepsilon_{si}\,N_A\,2\,\phi_b}}{C_{ox}} + V_{fb}.$$

$$V_{to} = 0.4 \text{ V}$$

For 180 nm process the oxide thickness $= 40 \times 10^{-8}$ cm.

$$\varepsilon_0 = 3.9$$

$$\varepsilon_{ins} = 8.85 \times 10^{-14} \text{ F/cm}$$

$$C_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_{ins}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{40 \times 10^{-8}}$$

$$= 8.62875 \times 10^{-7} \text{ F/cm}^2$$

$$\gamma = \frac{1}{0.862875 \times 10^{-5}} \sqrt{2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.85 \times 10^{-14} \times 8 \times 10^{17}}$$

$$= \frac{5.1485 \times 10^{-7}}{8.62875 \times 10^{-7}} = 0.596 \text{ V}^{1/2}$$

$$= .6 \text{ V}^{1/2}$$

$$\phi_b = \frac{KT}{q} \ln \frac{N_A}{N_i}$$

$$K = 1.380 \times 10^{-23} \text{ J/°K}$$

$$T = 300 \text{ °} K.$$

$$q = 1.6 \times 10^{-19} \text{ coulomb}$$

$$N_A = 8 \times 10^{17} \text{ cm}^{-3}$$

$$N_i = 1.45 \times 10^{10} \text{ cm}^{-3}$$

$$\phi_b = \frac{1.380 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \ln \left[\frac{8 \times 10^{17}}{1.45 \times 10^{10}} \right]$$

$$= .46 \text{ V}$$

$$V_t = .4 + .6 [\sqrt{2 \times .46 + 1.1} - \sqrt{2 \times .46}]$$

$$V_t = 0.68 \text{ V}$$

Problem 2: **Consider an n-channel MOSFET with the following characteristics: $t_{ox} = 10$ nm, $\mu_n = 520$ cm^2/V – sec, $\frac{W}{L} = 8$, $V_{tn} = .7V$, calculate the drain current for $V_{gs} = 2$ V and $V_{ds} = 1.2$ V, $V_{gs} = 2$ V and $V_{ds} = 2$ V.**

Solution:

$$t_{ox} = 10 \times 10^{-9} \text{ m} = 10 \times 10^{-7} \text{ cm.}$$

$$C_{ox} = \frac{\varepsilon_{ins} \cdot \varepsilon_0}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{10 \times 10^{-7}}$$

$$= 3.45 \times 10^{-7} \text{ F/cm}^2$$

The process transconductance $K = \mu_n \cdot C_{ox}$.

$$K = 520 \times 3.45 \times 10^{-7}$$

$$= 1.794 \times 10^{-4} \text{ A/V}^2$$

$$= 179 \, \mu \text{ A/V}^2$$

The device transconductance $\beta = K\left(\frac{W}{L}\right)$

$$\beta_n = 179 \times 10^{-6} \times 8 = 1.43 \text{ mA/V}^2$$

When $V_{gs} = 2$ V and $V_{ds} = 1.2$ V

$$V_{sat} = V_{gs} - V_{tn}$$

$$= 2 - .7$$

$$= 1.3 \text{ V}$$

$V_{ds} = 1.2 \text{ V} < V_{sat}$, which says the device operates in linear region, therefore the current

$$I_{ds} = \beta_n \left[V_{gs} - V_{tn} - \frac{V_{ds}}{2} \right] \times V_{ds}$$

$$= 1.43 \times 10^{-3} \, [2 - .7 - .6] \times 1.2$$

$$= 1.2 \text{ mA}$$

When $V_{gs} = 2$ V and $V_{ds} = 2$ V

$$V_{sat} = V_{gs} - V_{tn}$$

$$= 2 - .7$$

$$= 1.3 \text{ V}$$

Since $V_{ds} = 2\text{ V} > V_{sat}$, the device operates in saturated region. Therefore the current

$$I_{ds} = \frac{\beta_n}{2}\left[V_{gs} - V_{tn}\right]^2$$

$$= \frac{1.43}{2} \times 10^{-3}\,[2 - .7]^2$$

$$= 1.21\text{ mA}$$

Problem 5: **Calculate the drain current of silicon nMOS with $V_t = 1$ V, $W = 10\ \mu m$, $L = 1\ \mu m$ and $t_{ox} = 20nm$. The device is biased with $V_{gs} = 3$ V and $V_{ds} = 5$ V, with surface mobility of 300 cm^2/V. Sec and set $V_{bs} = 0V$. Also calculate the transconductance at $V_{gs} = 3$ V and $V_{ds} = 5$ V.**

Solution: The nMOS is biased in saturation since $V_{ds} > V_{gs} - V_t$

Therefore the drain current equals;

$$I_{ds} = \mu\, C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

where $\mu = 300\ cm^2/V - S$ (surface mobility)

$$W = 10\ \mu m\ ;\ L = 1\ \mu m\ ;\ C_{ox} = \frac{\varepsilon_0\, \varepsilon_{ins}}{t_{ox}}\ ; \varepsilon_0 = 8.85 \times 10^{-14}\ Fcm^{-1}\ ;\ \varepsilon_{ins} = 3.9 \text{ for silicon} - \text{dioxide}$$

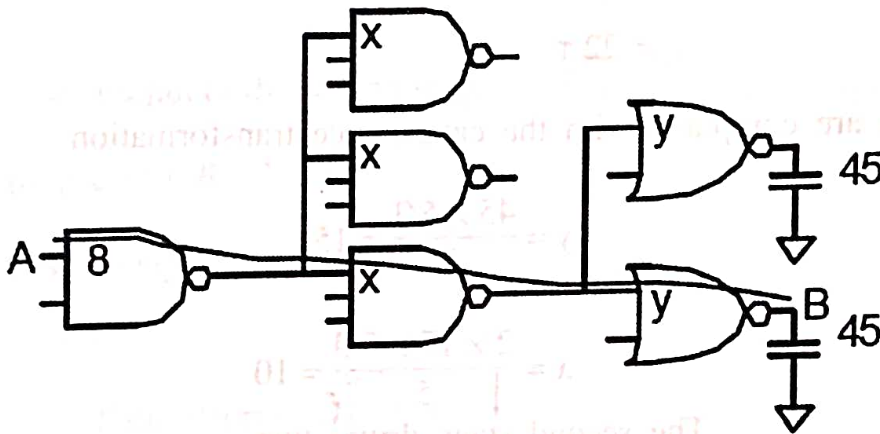
$$I_{ds} = 300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times \frac{(3-1)^2}{2} = 1.04\ mA$$

The transconductance equals:

$$g_m = \mu\, C_{ox} \frac{W}{L} (V_{gs} - V_t)$$

$$= 300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times (3 - 1) = 1.04$$

Problem 14: **Estimate the minimum delay of the path from A to B in the given Figure and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of 8λ of transistor width on the input and the output load is equivalent to 45λ of transistor width.**



Solution: The path logical effort along A to $B = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3}$

$$G = \frac{100}{27}.$$

The path electrical effort $H = \frac{45}{8}$

Branching effort $\quad B =$ The branching effort at the output of the first stage × the branching effort at the output of the second stage.

$$B = \left(\frac{x+x+x}{x}\right) \cdot \left(\frac{y+y}{y}\right)$$

$$B = \frac{3x}{x} \cdot \frac{2y}{y}$$

$$B = 3 \times 2 = 6$$

The path effort $F = GBH$

$$= \frac{100}{27} \times 6 \times \frac{45}{8} = 125$$

Best stage effort $\hat{f} = (F)^{1/N}$ $(N = 3)$

$$\hat{f} = (125)^{1/3}$$

$$\hat{f} = 5$$

Parasitic delay $P = 2 + 3 + 2 = 7$

2 ↑ 2 – i/p NAND; 3 ↑ 3 – i/p NAND; 2 ↑ 2 – i/p NOR

The minimum path delay $D = NF^{1/N} + P$

$$= 3 \times 5 \times 7$$

$$= 22\ \tau$$

The gate sizes are computed with the capacitance transformation

$$y = \frac{45 \times 5/3}{5} = 15$$

$$x = \frac{2 \times 15 \times 5/3}{5} = 10$$

↓ The second stage drives two copies of the third stage.

The ratio of P/N from stage A to B is shown below