Problem 7: Calculate the gate capacitance with an oxide capacitance of  $C_{ox} = 3.45 \times 10^{-7} \text{ F/cm}^2$  and a gate with dimensions  $W = 8 \mu \text{m}$  and  $L = .5 \mu \text{m}$ 

Solution:

$$C_g = C_{ox} \cdot A$$
 where  $A = WL$   
=  $3.45 \times 10^{-7} \times 8 \times 10^{-4} \times .5 \times 10^{-4}$   
=  $13.8 \times 10^{-15}$   
=  $13.8 \text{ fF}$ 

The gate-source and gate-drain contribution are then estimated by

$$C_{gs} = 1/2C_g$$
 and  $C_{gs} = 1/2C_g$  and  $C_{gs} = 1/2C_g$ 

Problem 11: Consider the nMOS transistor in a 180 nm process with a nominal therehold voltage of 0.4 V and doping level of  $8 \times 10^{17}$  cm<sup>-3</sup>. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1 V instead of 0 V?  $\varepsilon_{si} = 11.7 \times 8.85 \times 10^{-14}$  F/cm

Solution:  $V_{sb} = 1.1$ 

$$V_{sb} = 1.1$$

$$V_{t} = V_{to} + \gamma \left( \sqrt{2 \phi_{b} + |V_{sb}|} - \sqrt{2 \phi_{b}} \right)$$

$$V_{t} = \frac{1}{C_{ox}} \sqrt{2q \varepsilon_{si} \cdot N_{A}}$$

$$V_{t} = V_{to} + \gamma \left( \sqrt{2 \phi_{b} + |V_{sb}|} - \sqrt{2 \phi_{b}} \right)$$

$$V_{t} = V_{to} + \gamma \left( \sqrt{2 \phi_{b} + |V_{sb}|} - \sqrt{2 \phi_{b}} \right)$$

$$V_{to} = 2 \phi_b + \frac{\sqrt{2q \varepsilon_{si} N_A 2 \phi_b}}{C_{ox}} + V_{fb}.$$

Problem 12: Consider the nMOS transistor in a fl.o µm process with gate oxide thickness of 100 Å. The doping level is  $N_A = 3 \times 10^{17}$  cm<sup>-3</sup> and the  $1/0.0 \times 0.0 \times 10^{17}$  reshold voltage in

For 180 nm process the oxide thickness =  $40 \times 10^{-8}$  cm. request most be specified.

$$\varepsilon_0 = 3.9$$
 1.17 × 8.85 × 10  $^{-14}$  F/cm.

$$\varepsilon_{\text{ins}} = 8.85 \times 10^{-14} \text{ F/cm}$$

$$C_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_{\text{ins}}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-14}}{40 \times 10^{-8}}$$

$$= 8.62875 \times 10^{-7} \text{ F/cm}^2$$

d is the charge of an electron

4= C 1218 NA

$$= \frac{5.1485 \times 10^{-7}}{8.62875 \times 10^{-7}} = 0.596 \text{ V}^{1/2}$$

$$= .6 V^{1/2}$$

$$\phi_b = \frac{KT}{q} \ln \frac{N_A}{N_i}$$

$$K = 1.380 \times 10^{-23}$$
 J/°K in a nearly and to instance anticelable and is  $m^2$ 

$$T = 300 \circ K$$
. This depends consequently and the state of the state o

$$q = 1.6 \times 10^{-19}$$
 coulomb and unique from  $\sqrt{1.0}$  to again blooms  $N_A = 8 \times 10^{17}$  cm<sup>-3</sup>

$$N_A = 8 \times 10^{17} \text{ cm}^{-3}$$
 all adjacent door flow much vall being stratedus a dis

$$N_i = 1.45 \times 10^{10} \text{ cm}^{-3}$$

$$\phi_b = \frac{1.380 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \ln \left[ \frac{8 \times 10^{17}}{1.45 \times 10^{10}} \right]$$

$$= .46 \text{ V}$$

$$= .46 \, \text{V}$$

$$V_I = .4 + .6 \left[ \sqrt{2 \times .46 + 1.1} - \sqrt{2 \times .46} \right]$$

$$V_{t} = 0.68 \text{ V}$$

Consider an n-channel MOSFET with the following characteristics:  $t_{ox} = 10 \text{ nm}, \quad \mu_n = 520 \text{ cm}^2/\text{V} - \text{sec}, \quad \frac{W}{L} = 8, V_{tn} = .7V, \text{ calculate the drain current } t_{0r}$ 

 $V_{gs} = 2 \text{ V}$  and  $V_{ds} = 1.2 \text{ V}$ ,  $V_{gs} = 2 \text{ V}$  and  $V_{ds} = 2 \text{ V}$ . age against of merit in shows that the swinting spiral depends on the williage age

$$t_{ox} = 10 \times 10^{-5} \text{ m} = 10 \times 10^{-5} \text{ cm}.$$

$$t_{ox} = 10 \times 10^{-5} \text{ m} = 10 \times 10^{-5} \text{ cm}.$$

$$t_{ox} = \frac{\varepsilon_{ins} \cdot \varepsilon_{0}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{10 \times 10^{-7}} \approx 0) \text{ for an absence of single of sing$$

$$= 3.45 \times 10^{-7} \text{ F/cm}^2$$

The process transconductance  $K = \mu_n \cdot C_{ox}$ .

$$K = 520 \times 3.45 \times 10^{-7}$$
$$= 1.794 \times 10^{-4} \text{ A/V}^2$$
$$= 179 \text{ } \mu \text{ A/V}^2$$

observation of the state of the

 $C = 2.876 \times 10^{-7} \, \text{Pm}^2$ 

The process manaconductance  $K = \mu_B \cdot C_{av}$ 

For lot so mi (Axx = min 8 = 10) no

 $K = 540 \times 4.314 \times 10^{-7}$ 

If the oxide melanos, is reduced

The device transconductance  $\beta = K \left( \frac{W}{L} \right)$ For  $t_{ox} = 12 \text{ min} = 12 \times 10^{-9} \text{ m} = 1.2 \times 10^{-9}$  $\beta_n = 179 \times 10^{-6} \times 8 = 1.43 \text{ mA/V}^2$ 

When 
$$V_{gs} = 2 \text{ V}$$
 and  $V_{ds} = 1.2 \text{ V}$ 

$$V_{\text{sat}} = V_{gs} - V_{tn}$$
$$= 2 - \cdot 7$$
$$= 1.3 \text{ V}$$

 $V_{ds} = 1.2 \text{ V} < V_{\text{sat}}$ , which says the device operates in linear region, therefore the current

$$I_{ds} = \beta_n \left[ V_{gs} - V_{tn} - \frac{V_{ds}}{2} \right] \times V_{ds}$$
  
= 1.43 × 10<sup>-3</sup> [2 - .7 - .6] × 1.2  
= 1.2 mA

When  $V_{gs} = 2 \text{ V}$  and  $V_{ds} = 2 \text{ V}$ 

$$V_{
m sat} = V_{gs} - V_{tm}$$
 = 2 - .7

-- = 1.3 V propagate there is the propagate will be the state of the s

Since  $V_{ds} = 2 \text{ V} > V_{\text{sat}}$ , the device operates in saturated region. Therefore the current

$$I_{ds} = \frac{\beta_n}{2} \left[ V_{gs} - V_{tn} \right]^2$$
$$= \frac{1.43}{2} \times 10^{-3} \left[ 2 - .7 \right]^2$$
$$= 1.21 \text{ mA}$$

Problem 5: Calculate the drain current of silicon nMOS with  $V_t = 1$  V,  $W = 10 \, \mu m$ ,  $L = 1 \, \mu m$  and  $t_{ox} = 20 \, nm$ . The device is biased with  $V_{gs} = 3$  V and  $V_{ds} = 5$  V, with surface mobility of  $300 \, \text{cm}^2/V$ . Sec and set  $V_{bs} = 0$ V. Also calculate the transconductance at  $V_{gs} = 3$  V and  $V_{ds} = 5$  V.

Solution: The nMOS is biased in saturation since  $V_{ds} > V_{gs} - V_t$ 

Therefore the drain current equals;

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

where  $\mu = 300 \text{ cm}^2/V - S$  (surface mobility)

 $W = 10 \,\mu\text{m}$ ;  $L = 1 \,\mu\text{m}$ ;  $C_{ox} = \frac{\varepsilon_0 \,\varepsilon_{\text{ins}}}{t_{ox}}$ ;  $\varepsilon_0 = 8.85 \times 10^{-14} \,\text{Fcm}^{-1}$ ;  $\varepsilon_{ins} = 3.9 \,\text{for silicon} - \text{dioxide}$ 

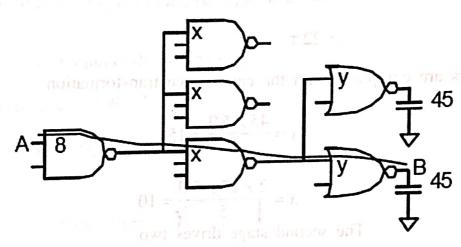
$$I_{ds} = 300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times \frac{(3-1)^2}{2} = 1.04 \text{ mA}$$

The transconductance equals:

$$g_m = \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)$$

$$=300 \times \frac{3.9 \times 8.85 \times 10^{-14}}{20 \times 10^{-7}} \frac{10}{1} \times (3-1) = 1.04$$

Problem 14: Estimate the minimum delay of the path from A to B in the given Figure and choose transistor sizes to achieve this delay. The initial NAND2 gate may present a load of  $8\lambda$  of transistor width on the input and the output load is equivalent to  $45\lambda$  of transistor width.



Solution: The path logical effort along A to  $B = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3}$ 

$$G=\frac{100}{27}.$$

The path electrical effort  $H = \frac{45}{8}$ 

Branching effort B = The branching effort at the output of the first stage  $\times$  the branching effort at the output of the second stage.

$$B = \left(\frac{x + x + x}{x}\right) \cdot \left(\frac{y + y}{y}\right)$$

$$B = \frac{3x}{x} \cdot \frac{2y}{y}$$

$$B = 3 \times 2 = 6$$

the electrical effort at stage 2 mg

The path logical effort

Middle Width.

The path effort F = GBH

$$= \frac{100}{27} \times 6 \times \frac{45}{8} = 125$$

Best stage effort  $\hat{f} = (F)^{1/N}$  (N = 3)

$$\hat{f} = (125)^{1/3}$$
 $\hat{f} = 5$ 

The minimum path delay  $D = NF^{1/N} + P$  begin on the rotation to A2 be to

$$= 3 \times 5 \times 7$$
$$= 22 \tau$$

The gate sizes are computed with the capacitance transformation

$$y = \frac{45 \times 5/3}{5} = 15$$

$$x = \frac{2 \times 15 \times 5/3}{5} = 10$$

The second stage drives two copies of the third stage.

The ratio of P/N from stage A to B is shown below

